said image acquisition portion integrated in said substrate including an array of active pixel type photoreceptors, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, wherein said array of photoreceptors are controlled to output an entire row of said photoreceptors substantially simultaneously; and

a plurality of double sampling charge storage elements integrated on said substrate; one for each of said columns.

51 (Amended) A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of active pixel type photoreceptors, where

each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, wherein said signal controlling device includes a column selector allowing selection of a desired column for read out, and a row selector which allows selection of a desired row fro readout.

14. (Amended) A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of

said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors,

wherein said signal controlling device includes a column selector allowing selection of a desired column for read out, and a row selector which allows selection of a desired row for readout,

wherein said row selector includes a latch element, storing a value for a row to be selected, and a counter, allowing incrementing of said value to read a next consecutive row, said latch element and said counter both being integrated on said substrate.

15. (Amended) A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, wherein said signal controlling device includes a column selector allowing selection of a desired column for read out, and a row selector which allows selection of a desired row for readout, wherein said column selector includes presettable start and stop column decoder counters, which are preset to start and stop at any desired value.

10. (Amended) A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, further comprising a mode selector device, selecting a mode of operation of said chip,

wherein said photoreceptors are either photogates or photodiodes, and said mode selector device selects a first mode of operation for operation with photogates, and second mode of operation, different that said first mode of operation, for operation with photodiodes.

17

23. (Amended) A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, and

further comprising a correlated double sampling circuit.

13. (Amended) A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors,

wherein said timing circuit controls readout from said chip in a correlated double sampling mode.

15 27 (Amended) A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, and

Attorney's Docket No.: 06816/019002/CIT2363

further comprising fixed pattern noise reduction circuits, on said substrate.

16 2) (Amended) A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

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said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors,

further comprising double delta sampling element integrated on the chip, which shorts sample signals during the readout cycle reducing column fixed pattern noise.

D6 cont 18 30.) (Amended) A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, further comprising a noise reduction circuit,

wherein said timing circuit times an operation of said noise reduction circuit to occur during a time of the video signal which is not being displayed.

16. (Amended) A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors arranged in rows and columns;

a charge storage element, associated with each said column;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors;

said control portion including common logic elements to control all pixels on a selected row to sample said all pixels onto said charge storage elements substantially simultaneously,

wherein said photoreceptors are either photogates or photodiodes, and said mode selector device selects a first mode of operation for operation with photogates, and a second mode of operation, different than said first mode of operation, for operation with photodiodes.